IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BOARD OF PATENT APPEALS AND INTERFERENCES

In re application of: Chaudhry et al.	§	
	§	
Serial Number: 10/759,936	§	
	§	Group Art Unit: 2128
Filed: January 16, 2004	§	
	§	
For: METHOD AND APPARATUS FOR VLSI CLOCK GATED POWER ESTIMATION USING LCB COUNTS	§	Examiner: Herng-der Day

Commissioner of Patents and Trademarks
P.O. Box 1450
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APPLICANTS' APPEAL BRIEF

Applicant-inventors ("Applicants") and assignee International Business Machines Corporation respectfully submit the present brief in support of the patentability of the claims of the above-referenced application.

I. REAL PARTY IN INTEREST

The real party in interest is International Business Machines Corporation, of Armonk, New York, assignee of the interests in the invention from the named inventors.

II. RELATED APPEALS AND INTERFERENCES

None.

III. STATUS OF CLAIMS

Claims 1-24 are pending. Of these, Claims 1, 9, and 17 are independent Claims. No Claims have been canceled. Applicants appeal the Examiner's rejections of Claims 1-24 under 35 U.S.C. §103(a) and 35 U.S.C. §112, first paragraph.

IV. STATUS OF AMENDMENTS

The Claims stand as amended in the Response to an Office Action dated March 5, 2007 ("First Response").

V. SUMMARY OF CLAIMED SUBJECT MATTER

Power consumption is a significant factor in very large-scale integration (VLSI) design, which aims to provide low-power integrated circuits (or "chips"). *See* Application, Page 1, lines 13-16. Typical power consumption approaches break a chip into smaller, more manageable analytic components, know as "macros." *See* Application, Page 1, lines 17-19. Typical approaches generate an energy model for each macro based on the input pins in consideration of clock activity and switching, among other factors. *See* Application, Page 2, lines 1-4.

In conventional algorithms, however, system clocks are assumed at one hundred percent activity (*i.e.*, always ON), which leads to a maximal power assessment. *See* Application, Page 2, lines 4-8. This maximal power assessment of the conventional approaches leads to inherent

inaccuracies in the resultant energy model, in part because the model does not accurately account for real operational behavior. *See* Application, Page 2, lines 12-19.

The present invention, defined in Claims 1-24, solves these and other problems by providing a novel method and apparatus for generating circuit energy models that represent operational behavior, and are therefore better suited to subsequent use in the system design process. Generally, the method approximates power consumption of a circuit with a plurality of local clock buffers (LCBs). *See* Application, Page 10, lines 9-11.

A Hardware Descriptive Language (HDL) simulator data of the circuit is inputted into a power modeler. *See* Application, Page 15, lines 15-18. Net capacitance data of the circuit is inputted into the power modeler. *See* Application, Page 15, lines 15-18. Energy model data is inputted into the power modeler. *See* Application, Page 15, lines 15-18. The energy model data further comprises extrapolating energy data by increasing or decreasing the number of active LCBs. *See* Application, Page 14, line 5 to Page 15, line 10. Power consumption data is generated from the HDL simulator data, the net capacitance data, and the energy model data. *See* Application, Page 16, lines 18-22. An operational model based on the generated power consumption data is stored for subsequent use. *See* Application, Page 10, lines 4-8; Page 15, lines 18-22; and Page 16, lines 18-22.

This novel approach offers several advantages that are unavailable to the prior art methods or systems. This novel approach avoids the miscalculations of prior approaches. *See* Application, Page 2, lines 12-19. The unique combination recited in the pending Claims also yields an improved power consumption model that reflects the activation of a fraction of the total number of active clock signals. *See* Application, Page 9, lines 7-9. Other advantages will be highlighted as necessary below.

The Claims embody the invention as follows, shown with illustrative citations to page and line numbers in the Original Application designated in curved braces ("{}"):

1. (Previously Presented) A method for approximating power consumption of a circuit with a plurality of local clock buffers (LCBs), {Page 10, lines 9-11} comprising:

inputting a Hardware Descriptive Language (HDL) simulator data of the circuit; {Page 15, lines 15-18}

inputting net capacitance data of the circuit; {Page 15, lines 15-18}

inputting energy model data {Page 15, lines 15-18}, wherein the energy model data further comprises extrapolating energy data by increasing or decreasing the number of active LCBs; {Page 14, line 5 to Page 15, line 10}

generating power consumption data from the HDL simulator data, the net capacitance data, and the energy model data; and {Page 16, lines 18-22}

storing, for subsequent use, an operational model based on the generated power consumption data. {Page 10, lines 4-8; Page 15, lines 18-22; and Page 16, lines 18-22}

9. (Previously Presented) An apparatus for approximating power consumption of a circuit with a plurality of local clock buffers (LCBs), {Page 10, lines 9-11} comprising:

means for inputting HDL simulator data of the circuit; {Page 15, lines 15-18}

means for inputting net capacitance data of the circuit; {Page 15, lines 15-18}

means for inputting energy model data {Page 15, lines 15-18}, wherein the energy model data further comprises extrapolating energy data by increasing or decreasing the number of active LCBs; {Page 14, line 5 to Page 15, line 10}

means for generating power consumption data from the HDL simulator data, the net capacitance data, and the energy model data; and {Page 16, lines 18-22}

means for storing, for subsequent use, an operational model based on the generated power consumption data. {Page 10, lines 4-8; Page 15, lines 18-22; and Page 16, lines 18-22}

17. (Previously Presented) A computer program product for approximating power consumption of a circuit with a plurality of local clock buffers (LCBs), {Page 10, lines 9-11} the computer program product having a medium with a computer program embodied thereon, the computer program comprising:

computer code for inputting HDL simulator data of the circuit; {Page 15, lines 15-18}

computer code for inputting net capacitance data of the circuit; {Page 15, lines 15-18}

computer code for inputting energy model data {Page 15, lines 15-18}, wherein the energy model data further comprises extrapolating energy data by increasing or decreasing the number of active LCBs; {Page 14, line 5 to Page 15, line 10}

computer code for generating power consumption data from the HDL simulator data, the net capacitance data, and the energy model data; and {Page 16, lines 18-22}

computer code for storing, for subsequent use, an operational model based on the generated power consumption data. {Page 10, lines 4-8; Page 15, lines 18-22; and Page 16, lines 18-22}

VI. GROUNDS OF REJECTION TO BE REVIEWED

A. Whether Claims 1-24 are sufficiently enabled in the Application.

B. Whether Claims 1-24 are patentable over Radjassamy in view of Lim.

VII. ARGUMENT

A. Grouping of Claims

Claims 1, 9, and 17 are independent. For purposes of this appeal, Applicants consider each of the independent Claims, and their respective dependent Claims, as separate groups. Thus, the groups of Claims are 1-8, 9-16, and 17-24.

B. Summary of Pertinent Prosecution

Applicants filed the present application on January 16, 2004, with 24 claims.

The Examiner mailed the first Office Action on December 5, 2006 ("First Action"), rejecting Claims 1-24 under 35 U.S.C. §103(a) as allegedly unpatentable over Radjassamy (U.S. Pat. App. Pub. No. 2004/0186703 A1)("Radjassamy") in view of Lim et al. (U.S. Pat. No. 5,481,209)("Lim").

Claim 21 was also rejected under 35 U.S.C. §101 as allegedly directed to non-statutory subject matter. In particular, the Examiner stated that the claims "appear to be directed merely to the manipulation of an abstract idea of approximating power consumption of a circuit with [sic] plurality of local clock buffers (LCBs) without resulting in a practical application producing a concrete, useful, and tangible result." First Action, Page 4.

The Examiner also rejected Claims 14-16 under 35 U.S.C. §112, first paragraph for insufficient antecedent basis in reciting "The method."

On March 2, 2007, Applicants' representative and the Examiner held a telephone interview ("Telephone Interview") to discuss an amendment to overcome the Examiner's rejections, in particular the rejections under Section 101. During the interview, the Examiner

and Applicants' representative agreed on the following claim language: "storing, for subsequent use, an operational model based on the generated power consumption data" to overcome the Section 101 rejection.

Applicants responded to the first Office Action on March 5, 2007 ("First Response"), amending Claims 1, 9, and 14-17 to overcome the Examiner's rejections, in accordance with the Telephone Interview. Applicants also argued against the Examiner's rejections under Section 103.

The Examiner mailed the Final Action under appeal on May 18, 2007 ("Final Action"), sustaining the First Action's Section 103 rejection. The Examiner withdrew the rejection under Section 101 and the original Section 112 rejection, but added a new rejection under Section 112, first paragraph, asserting that "storing, for subsequent use, an operational model" does not appear to have support in the original disclosure. Final Action, Page 2. The Examiner also responded to Applicants' arguments of the First Response. This appeal followed.

C. The Examiner's Rejections Were Procedurally and Factually in Error

1. The Form and Content of the Examiner's Rejections under Section 112, First Paragraph, Were Improper and Insufficient

a. Legal Requirements for a Written Description Rejection

The "written description requirement" refers to the statutory requirement that the Specification include "a written description of the invention." *See* M.P.E.P. §2161; 35 U.S.C. §112, 1st paragraph. Because the purpose of the written description is to ensure that the inventor(s) had possession of the claimed subject matter as of the filing date of the application, how the Specification accomplishes the written description is immaterial. *See* M.P.E.P. §2161 (*citing In re Herschler*, 591 F.2d 693, 700-01, 200 USPQ 711, 717 (CCPA 1979) and *In re Kaslow*, 707 F.2d 1366, 707 F.2d 1366, 217 USPQ 1089 (Fed. Cir. 1983)), §2163 *et seq*.

The appropriate test for analyzing whether the Specification satisfies the written description requirement is whether the Specification describes "the claimed invention in sufficient detail that one skilled in the art can reasonably conclude that the inventor had possession of the claimed invention." M.P.E.P. §2163(I) (citing *Moba, B.V. v. Diamond Automation, Inc.*, 325 F.3d 1306, 1319, 66 USPQ2d 1429, 1438 (Fed. Cir. 2003); *Vas-Cath, Inc. v. Mahurkar*, 935 F.2d at 1563, 19 USPQ2d at 1116).

Ordinarily, especially in the claims as filed, an "applicant shows possession of the claimed invention by describing the claimed invention with all of its limitations using such descriptive means as words, structures, figures, diagrams, and formulas that fully set forth the claimed invention." M.P.E.P. §2161(I)(*citing Lockwood v. American Airlines, Inc.,* 107 F.3d 1565, 1572, 41 USPQ2d 1961, 1966 (Fed. Cir. 1997)). However, possession may be shown in a variety of ways and because "there is no *in haec verba* requirement," claim limitations not included in the original claims can be supported in the Specification through express, implicit, or inherent disclosure. *See* M.P.E.P. §2161(I)(B).

MPEP Section 2163 also sets forth a framework to establish which party has the burden of proof in written description requirement questions:

> If applicant amends the claims and points out where and/or how the originally filed disclosure supports the amendment(s), and the examiner finds that the disclosure does not reasonably convey that the inventor had possession of the subject matter of the amendment at the time of the filing of the application, the examiner has the initial burden of presenting evidence or reasoning to explain why persons skilled in the art would not recognize in the disclosure a description of the invention defined by the claims.

M.P.E.P. §2163(II)(A) (quoting §2163.04). Applicants respectfully submit that this framework is the appropriate one in this case.

b. The Examiner's Stated Grounds Were Insufficient

Applicants respectfully submit that the Examiner's stated grounds for a rejection based on the written description requirement were insufficient. Specifically, the Examiner failed to meet his burden to show why "persons skilled in the art would not recognize in the disclosure a description of the invention defined by the claims" as required under M.P.E.P. §2163(II)(A). *See also* M.P.E.P. §2163.04.

As described above, the appropriate framework in this case applies when an applicant has amended the claims to include the contested matter. *See* M.P.E.P. §2163(II)(A). In this case, Applicants amended Claims 1, 9, and 17 in the First Response to recite, "storing, for subsequent use, an operational model based on the generated power consumption data." *See* First Response, Pages 4-5.

Having amended the Claims, Applicants also pointed out "where and/or how the originally filed disclosure supports the amendment(s)" as required under M.P.E.P. §2163(II)(A). Specifically, Applicants discussed these amendments with the Examiner in the Telephone Interview. Moreover, Applicants also respectfully submit that support for these amendments can be found, among other places, at Page 10, lines 4-8 and Page 15, lines 18-22 of the Original Application.

Additionally, Applicants further respectfully submit that "storing, for subsequent use" is well-known in the art. In particular, as stated in the Original Application, "Examining smaller components of a chip allow for convenience in modeling. . . There are also a variety of simulator software packages that can be used to construct circuits, for example Simulated Program for Integrated Circuits Emphasis (SPICE)." Application, Page 1, lines 22-26. Applicants respectfully submit that one skilled in the art would understand that programs such as SPICE use models that have been stored for subsequent use.

Accordingly, having pointed to support in the Application, the burden shifts to the Examiner to show "why persons skilled in the art would not recognize in the disclosure a description of the invention defined by the claims." M.P.E.P. §2163(II)(A). The Examiner has also accepted this burden by stating that the Claims allegedly "contains subject matter which was not described in the specification in such as way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention." Final Action, Page 2. Applicants respectfully note that this is precisely the finding stated in the M.P.E.P. that shifts the burden to the Examiner. *See* M.P.E.P. §2163(II)(A).

And here, Applicants respectfully submit, is where the Examiner failed to meet his burden. In particular, the Examiner failed to show, or even suggest, how or why persons skilled in the art would not recognize in the disclosure a description of the invention defined by the claims. Instead, the Examiner restated his finding that "'storing, for subsequent use, an operational model' does not appear to have support in the original disclosure." Final Action, Page 2. As further evidence, the Examiner even restated the restated finding, "In other words, no evidence in the original disclosure can be found to support the added limitation." Final Action, Page 2.

As such, Applicants respectfully submit that the Examiner has himself stated that the test he used was not "why persons skilled in the art would not recognize in the disclosure a description of the invention defined by the claims" but instead whether there is "support" in the original disclosure. Applicants respectfully submit that these two approaches are fundamentally different.

First, as described above, Applicants need not use the exact language of the Claims in the disclosure or even *expressly* support the Claim limitations. Instead, possession of the claimed

invention at filing may be shown in a variety of ways and because "there is no *in haec verba* requirement," claim limitations not included in the original claims can also be supported in the Specification through *implicit* or *inherent* disclosure. *See* M.P.E.P. §2161(I)(B). But the statement that a element "does not appear to have support in the original disclosure" can only describe a lack of express support. The appropriate test instead queries whether "persons skilled in the art would not recognize in the disclosure" support, which is a standard that does include implicit and inherent disclosure.

Second, the difference between the two approaches is, in this case, the difference between compliance and non-compliance. Under the Examiner's approach, the simple failure to state "storing, for subsequent use, an operational model" results in non-compliance. However, Applicants respectfully submit that had the Examiner actually considered whether persons skilled in the art would find support, there would be no need for Applicants to appeal this point.

That is, as mentioned above, Applicants respectfully submit that the Original Application provides sufficient teaching to support the claimed limitations, as recognized by one skilled in the art. Specifically, the Specification states, "Examining smaller components of a chip allow for convenience in modeling. . . There are also a variety of simulator software packages that can be used to construct circuits, for example Simulated Program for Integrated Circuits Emphasis (SPICE)." Application, Page 1, lines 22-26. Applicants respectfully submit that one skilled in the art would understand that programs such as SPICE use models that have been stored for subsequent use. That is, it is inherent in the programs and software packages that use circuit models, which includes operational models, to use models that have been stored for subsequent use. As such, one skilled in the art would therefore recognize in the disclosure a description of

the invention defined by the Claims, and in particular "storing, for subsequent use, an operational model based on the generated power consumption data," as recited in Claims 1, 9, and 17.

Therefore, for at least the above reasons, Applicants respectfully submit that the Examiner has failed to meet his burden as required under the M.P.E.P. Further, Applicants respectfully submit that even had the Examiner applied the appropriate test, the Claims as amended are supported by the disclosure in such a way as to satisfy the requirements of Section 112, first paragraph.

Accordingly, Applicants respectfully submit that the Examiner's rejections are in error and should be withdrawn.

2. The Form and Content of the Examiner's Rejections under Section 103 Were Improper and Insufficient

a. Legal Requirements for an Obviousness Rejection

The obligation of the examiner to produce reasoning and evidence in support of obviousness is clearly defined at M.P.E.P. §2142:

> The examiner bears the initial burden of factually supporting any *prima facie* conclusion of obviousness. If the examiner does not produce a *prima facie* case, the applicant is under no obligation to submit evidence of nonobviousness.

M.P.E.P. §2143 sets out the three basic criteria that a patent examiner must satisfy to establish a *prima facie* case of obviousness:

> 1. some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings;
> 2. a reasonable expectation of success; and
> 3. the teaching or suggestion of all the claim limitations by the prior art reference (or references when combined).

It follows that in the absence of such a *prima facie* showing of obviousness by the Examiner (assuming there are no objections or other grounds for rejection), an applicant is entitled to grant of a patent. *In re Oetiker*, 977 F.2d 1443, 1445, 24 USPQ2d 1443 (Fed. Cir.

1992). Thus, in order to support an obviousness rejection, the Examiner is obliged to produce evidence compelling a conclusion that each of the three aforementioned basic criteria has been met.

b. The Examiner's Stated Grounds Were Insufficient

As described above, the Examiner in the Final Action rejects Claims 1-24 under 35 U.S.C. §103(b) as allegedly unpatentable over Radjassamy in view of Lim. Applicants respectfully submit that these rejections are in error and should be withdrawn.

In this case, Applicants respectfully submit that the Examiner has failed to produce evidence compelling a conclusion that the criteria required for a *prima facie* showing of obviousness has been met. In particular, the Examiner admits that "Radjassamy fails to expressly disclose wherein the energy model data further comprises extrapolating energy data by increasing or decreasing the number of active LCBs," as recited in independent Claims 1, 9, and 17. Final Action, Page 4.

To supply this admittedly missing element, the Examiner offers Lim, which allegedly discloses "an apparatus and method for improved clock distribution and control in an integrated circuit having the ability to selectively inhibit clock signals at the local buffer 46." Final Action, Page 4. Moreover, the Examiner asserts that "Using inhibit 52 to inhibit the clock at selected locations of the integrated circuit 10 allows for reduction of power dissipation." Final Action, Page 4 (*citing* Lim, col. 4, lines 62-67). Further, the Examiner states, "It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Radjassamy to incorporate the teachings of Lim et al. to obtain the invention as specified in claim 1 because inhibiting locally buffered clock signals at selected locations results in reduced power dissipation as suggested by Lim et al." Final Action, Page 4. Applicants respectfully disagree with the Examiner's assertion.

Specifically, Applicants respectfully note that the examiner offers Lim as showing "inhibiting the clock at selected locations" to allow for "reduction of power dissipation." But the Examiner cannot show anywhere in Lim where Lim even hints at "reduced *estimation* of power dissipation." Instead, Lim teaches using LCBs to reduce actual power dissipation, not an estimated power dissipation, and certainly not "extrapolating energy data by increasing or decreasing the number of active LCBs," as recited in the Claims. Lim expressly teaches, "Inhibiting the clock at selected locations of the integrated circuit allows for *reduction of power dissipation*, and specific logical operations involving only part of the integrated circuit chip logic." Lim, col. 3, lines 19-22. Nowhere does Lim come anywhere close to teaching, "extrapolating energy data by increasing or decreasing the number of active LCBs," as recited in the Claims.

The Examiner argues that because Radjassamy does teach estimating power consumption, it would have been obvious "to incorporate Lim's teaching in estimating power consumption." Final Action, Page 8. Applicants respectfully disagree because Radjassamy teaches away from combination with Lim, and therefore it cannot be said to be obvious to form the combination.

More particularly, there is no motivation to combine the Radjassamy system with Lim, as Radjassamy teaches away from "extrapolating energy data by increasing or decreasing the number of active LCBs," as recited in the Claims. Instead, Radjassamy teaches a power consumption correction factor called a "reduction factor":

> The power consumption may be estimated by way of one or more equations that include a raw power factor and a reduction factor for each power consumption component that is representative of a probabilistic activity profile associated with the power consumption component. . . [T]he probabilistic activity profile may comprise at least one activity factor that may take the form of a correction coefficient that is based on either the power consumption component's structural constraints, functional constraints, design constraints, process constraints, or some combination thereof. Accordingly, the reduction factor generator 218 employs

> one or more power consumption component's restraints to arrive at an activity factor profile for the component that represents the probabilistic reality of the way its circuitry is designed to operate under normal conditions.
>
> Radjassamy, Paragraph [0025].

As for latch arrays, for example, Radjassamy applies this reduction factor as follows: "the reduction factor may be based on a probabilistic activity profile comprising activity factors that characterize the particular component constraints such as the particular inputs and assertions of the latch array." Radjassamy, Paragraph [0076.] This is clearly a very different approach than "extrapolating energy data by increasing or decreasing the number of active LCBs," as recited in the Claims. Therefore, even if Lim did teach this element, which it does not, Radjassamy clearly rejects it in favor of another approach. For at least this reason, there is no motivation to combine Radjassamy with Lim, and therefore the Examiner's purported *prima facie* case must fail.

The Examiner argues that the above analysis constitutes an impermissible attack of the references individually. Final Action, Page 7 (*citing In re Keller*, 642 F.2d 413, 2108 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986)). Applicants respectfully disagree, in particular as it relates to references that affirmatively teach away from combination with each other, and in other circumstances.

For example, there are already several known circumstances wherein an Applicant may attack a reference individually. First, where "the teachings of two or more prior art references conflict, the examiner must weigh the power of each reference to suggest solutions to one of ordinary skill in the art, considering the degree to which one reference might accurately discredit another." M.P.E.P. §2143.01(II)(*citing In re Young*, 927 F.2d 588, 18 USPQ2d 1089 (Fed. Cir. 1991)). Second, if "proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the

proposed modification." M.P.E.P. §2143.01(V)(*citing In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984)).

And third, if "the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious." M.P.E.P. §2143.01(VI)(*citing In re Ratti*, 270 F.2d 810, 123 USPQ 349 (CCPA 1959)). Applicants respectfully submit that this is just what the Examiner attempts to do in modifying Radjassamy with Lim, as described above. Accordingly, Applicants have not impermissibly attacked the references individually. As such, Applicants respectfully submit that the Examiner's argument fails.

Therefore, for at least the above reasons, Applicants respectfully submit that the Examiner's proposed combination fails to teach each and every element as recited in the Claims, and fails for lack of motivation. Applicants therefore also respectfully submit that amended Claims 1, 9, and 17, and their dependent Claims, are therefore allowable over the cited art and the remaining art of record, in any combination.

For at least the above reasons, Applicants respectfully submits that the Examiner's proposed combination based on Radjassamy and Lim fails to teach or disclose all of the elements and limitations of Claims 1-24 and is therefore in error and must be withdrawn. As such, Applicants respectfully submit that Claims 1-24 are fully allowable in view of Radjassamy and Lim and should be allowed.

Accordingly, Applicants respectfully submit that the Examiner's stated grounds are insufficient to maintain the Final Rejections. Applicants therefore respectfully request that the Final Rejections be withdrawn and that Claims 1-24 be allowed.

VIII. CLAIMS APPENDIX

See Attached.

IX. EVIDENCE APPENDIX

NONE.

X. RELATED PROCCEDINGS APPENDIX

NONE.

XI. CONCLUSION

For the foregoing reasons, it is respectfully submitted that the Final Rejections of Claims 1-24 under 35 U.S.C. §103(a) and 35 U.S.C. §112, first paragraph, are improper and should be reversed. Applicants respectfully request that the rejections of Claims 1-24 be withdrawn and that Claims 1-24 be allowed.

Respectfully submitted,

Dated: October 22, 2007

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VIII – APPENDIX – CLAIMS ON APPEAL

1. (Previously Presented) A method for approximating power consumption of a circuit with a plurality of local clock buffers (LCBs), comprising:

inputting a Hardware Descriptive Language (HDL) simulator data of the circuit;

inputting net capacitance data of the circuit;

inputting energy model data, wherein the energy model data further comprises extrapolating energy data by increasing or decreasing the number of active LCBs;

generating power consumption data from the HDL simulator data, the net capacitance data, and the energy model data; and

storing, for subsequent use, an operational model based on the generated power consumption data.

2. (Original) The method of Claim 1, wherein each LCB of the plurality of LCBs is at least configured to consume the same amount of power.

3. (Original) The method of Claim 2, wherein the energy model data further comprises extrapolating energy data by increasing or decreasing numbers of active input signals to the circuit.

4. (Original) The method of Claim 1, wherein the method further comprises inputting template data, wherein the template data is at least configured to contain relative power consumption data for each LCB of the plurality of LCBs.

5. (Original) The method of Claim 4, wherein the relative power consumption data of each LCB of the plurality of LCBs are at least configured to be the same or different.

6. (Original) The method of Claim 5, wherein each LCB of the plurality of LCBs is at least configured to consume the same amount of power.

7. (Original) The method of Claim 6, wherein the energy model data further comprises extrapolating energy data by increasing or decreasing numbers of active input signals to the circuit.

8. (Original) The method of Claim 7, wherein the generating power consumption data is at least configured to utilize the template data.

9. (Previously Presented) An apparatus for approximating power consumption of a circuit with a plurality of local clock buffers (LCBs), comprising:

means for inputting HDL simulator data of the circuit;

means for inputting net capacitance data of the circuit;

means for inputting energy model data, wherein the energy model data further comprises extrapolating energy data by increasing or decreasing the number of active LCBs;

means for generating power consumption data from the HDL simulator data, the net capacitance data, and the energy model data; and

means for storing, for subsequent use, an operational model based on the generated power consumption data.

10. (Original) The apparatus of Claim 9, wherein each LCB of the plurality of LCBs is at least configured to consume the same amount of power.

11. (Original) The apparatus of Claim 10, wherein the energy model data further comprises means for extrapolating energy data by increasing or decreasing numbers of active input signals to the circuit.

12. (Original) The apparatus of Claim 9, wherein the method further comprises means for inputting template data, wherein the template data is at least configured to contain relative power consumption data for each LCB of the plurality of LCBs.

13. (Original) The apparatus of Claim 12, wherein the relative power consumption data of each LCB of the plurality of LCBs are at least configured to be the same or different.

14. (Previously Presented) The apparatus of Claim 13, wherein each LCB of the plurality of LCBs is at least configured to consume the same amount of power.

15. (Previously Presented) The apparatus of Claim 14, wherein the energy model data further comprises means for extrapolating energy data by increasing or decreasing numbers of active input signals to the circuit.

16. (Previously Presented) The apparatus of Claim 15, wherein the means for generating power consumption data is at least configured to utilize the template data.

17. (Previously Presented) A computer program product for approximating power consumption of a circuit with a plurality of local clock buffers (LCBs), the computer program product having a medium with a computer program embodied thereon, the computer program comprising:

computer code for inputting HDL simulator data of the circuit;

computer code for inputting net capacitance data of the circuit;

computer code for inputting energy model data, wherein the energy model data further comprises extrapolating energy data by increasing or decreasing the number of active LCBs;

computer code for generating power consumption data from the HDL simulator data, the net capacitance data, and the energy model data; and

computer code for storing, for subsequent use, an operational model based on the generated power consumption data.

18. (Original) The computer program product of Claim 17, wherein each LCB of the plurality of LCBs is at least configured to consume the same amount of power.

19. (Original) The computer program product of Claim 18, wherein the energy model data further comprises computer code for extrapolating energy data by increasing or decreasing numbers of active input signals to the circuit.

20. (Original) The computer program product of Claim 17, wherein the method further comprises computer code for inputting template data, wherein the template data is at least configured to contain relative power consumption data for each LCB of the plurality of LCBs.

21. (Original) The computer program product of Claim 20, wherein the relative power consumption data of each LCB of the plurality of LCBs are at least configured to be the same or different.

22. (Original) The computer program product of Claim 21, wherein each LCB of the plurality of LCBs is at least configured to consume the same amount of power.

23. (Original) The computer program product of Claim 22, wherein the energy model data further comprises computer code for extrapolating energy data by increasing or decreasing numbers of active input signals to the circuit.

24. (Original) The computer program product of Claim 23, wherein the generating power consumption data is at least configured to utilize the template data.